METHOD FOR MAKING PROGRAMMABLE RESISTANCE MEMORY ELEMENT

Related Application Information

This application is a continuation-in-part of U.S. Patent Application Serial Number 09/813,267 filed on March 20, 2001. This application is also a continuation-in-part of U.S. Patent Application Serial Number 09/677,957 filed on October 3, 2000. This application is also a continuation-in-part of U.S. Patent Application Serial Number 09/620,318 filed on July 22, 2000. This application is also a continuation-in-part of U.S. Patent Application Serial Number 09/276,273 filed on March 25, 1999.

Field of the Invention

The present invention relates generally to electrically operable memory elements. More specifically, the present invention relates to programmable resistance memory elements.

Background and Prior Art

Programmable resistance memory elements formed from materials that can be programmed to exhibit at least a high or low stable ohmic state are known in the art. Such programmable resistance elements may be programmed to a high resistance state to store, for example, a logic ONE data bit. As well, they may be programmed to a low resistance state to store, for example, a logic ZERO data bit.

One type of material that can be used as the memory material for programmable resistance elements is phase change material.

Phase change materials may be programmed between a first structural state where the material is generally more amorphous (less ordered) and a second structural state where the material is generally more crystalline (more ordered). The term "amorphous", as used herein, refers to a condition which is relatively structurally less ordered or more disordered than a single crystal and has a detectable characteristic, such as high electrical resistivity. The term "crystalline", as used herein, refers to a condition which is relatively structurally more ordered than amorphous and has lower electrical resistivity than the amorphous state.

The concept of utilizing electrically programmable phase change materials for electronic memory applications is disclosed, for example, in U.S. Patent Nos. 3,271,591 and 3,530,441, the contents of which are incorporated herein by reference. The early phase change materials described in the '591 and '441 Patents were based on changes in local structural order. The changes in structural order were typically accompanied by atomic migration of certain species within the material. Such atomic migration between the amorphous and crystalline states made programming energies relatively high.

The electrical energy required to produce a detectable change in resistance in these materials was typically in the range of about a microjoule. This amount of energy must be delivered to each of the memory elements in the solid state matrix of rows and

columns of memory cells. Such high energy requirements translate into high current carrying requirements for the address lines and for the cell isolation/address device associated with each discrete memory element.

The high energy requirements for programming the memory cells described in the '591 and '441 patents limited the use of these cells as a direct and universal replacement for present computer memory applications, such as tape, floppy disks, magnetic or optical hard disk drives, solid state disk flash, DRAM, SRAM, and socket flash memory. In particular, low programming energy is important when the EEPROMs are used for large-scale archival storage. Used in this manner, the EEPROMs would replace the mechanical hard drives (such as magnetic or optical hard drives) of present computer systems. One of the main reasons for this replacement of conventional mechanical hard drives with EEPROM "hard drives" would be to reduce the power consumption of the mechanical systems. In the case of lap-top computers, this is of particular interest because the mechanical hard disk drive is one of the largest power consumers therein. Therefore, it would be advantageous to reduce this power load, thereby substantially increasing the operating time of the computer per charge of the power cells. However, if the EEPROM replacement for hard drives has high programming energy requirements (and high power requirements), the power savings may be inconsequential or at best unsubstantial. Therefore, any EEPROM which is to be considered a

universal memory requires low programming energy.

The programming energy requirements of a programmable resistance memory element may be reduced in different ways. For example, the programming energies may be reduced by the appropriate selection of the composition of the memory material. An example of a phase change material having reduced energy requirements is described in U.S. Patent No. 5,166,758, the disclosure of which is incorporated by reference herein. Other examples of memory materials are provided in U.S. Patent Nos. 5,296,716, 5,414,271, 5,359,205, and 5,534,712 disclosures of which are all incorporated by reference herein.

The programming energy requirement may also be reduced through the appropriate modification of the electrical contacts used to deliver the programming energy to the memory material. For example, reduction in programming energy may be achieved by modifying the composition and/or shape and/or configuration (positioning relative to the memory material) of the electrical contacts. Examples of such "contact modification" are provided in U.S. Patent Nos. 5341,328, 5,406,509, 5,534,711, 5,536,947, 5,687,112, 5,933,365 all of which are incorporated by reference herein. Examples are also provided in U.S. Patent Application Serial No. 09/276,273 the disclosure of which is incorporated herein by reference. Examples are also provided in U.S. Patent Application Serial No. 09/620,318 the disclosure of which is incorporated herein by reference. More examples are provided in

U.S. Patent Application Serial No. 09/677,957 the disclosure of which is incorporated herein by reference. Yet other examples are provided in U.S. Patent Application Serial No. 09/813,267 the disclosure of which is incorporated herein by reference. The present invention is directed to novel structures of a programmable resistance memory element and methods for making these structures.

Summary of the Invention

One aspect of the present invention A method for making a programmable resistance memory element, comprising: providing a conductive material; forming a sidewall spacer over a portion of the conductive material; removing a portion of the conductive material to form a raised portion extending from the conductive material under the spacer; and forming a programmable resistance material adjacent to at least a portion of the raised portion.

Another aspect of the invention is A method for making a programmable resistance memory element, comprising: providing a conductive layer; forming a raised portion extending from an edge of the conductive layer; and forming a programmable resistance material adjacent to at a least a portion of the raised portion.

Another aspect of the invention is A method of forming a programmable resistance memory element, comprising: providing a first dielectric layer; forming a sidewall surface in the dielectric layer; forming a conductive layer on the sidewall

surface; forming a second dielectric layer over the conductive layer; forming or exposing an edge of the conductive layer; forming a raised portion extending from the edge of the conductive layer; and forming a programmable resistance material adjacent to at least a portion of the raised portion.

Another aspect of the invention is A method for making an electrode for a semiconductor device, comprising: providing a conductive layer; and forming a raised portion extending from an edge of the conductive layer.

Another aspect of the invention is A method of making an electrode for a semiconductor device, comprising: providing a first dielectric layer; forming a sidewall surface in the dielectric layer; forming a conductive layer on the sidewall surface; forming a second dielectric layer over the conductive layer; forming or exposing an edge of the conductive layer; and forming a raised portion extending from the edge of the conductive layer.

Brief Description of the Drawings

Figure 1A is a cross sectional view of a memory device comprising conductive sidewall spacers as electrical contacts;

Figure 1B is a three-dimensional view of the conductive sidewall spacers shown in Figure 1A;

Figure 1C is a cross-sectional view, parallel to the y-z plane, of a memory element using conductive sidewall spacers with

rapier modification;

Figure 1D is a three-dimensional view of conductive sidewall spacers with rapier modification;

Figures 2A-2S shows a process for making the memory element of Figure 1C;

Figure 3A is a three-dimensional view of a memory device having a cylindrically shaped conductive sidewall spacer as an electrical contact;

Figure 3B is a three-dimensional view of cylindrically shaped conductive sidewall spacer with raised portions extending from the top edge of the sidewall spacer;

Figure 3C is a side view of a memory element using the electrical contact from Figure 3B;

Figure 4A is a conductive liner formed in a trench;

Figure 4B is a conductive liner formed in a rectangular opening;

Figure 4C is a conductive liner formed in a circular opening;

Figure 5A is a three-dimensional view of a memory device using a conductive liner as an electrical contact;

Figure 5B is a cross-sectional view of the memory device of Figure 5A;

Figure 5C is a three-dimensional view of a cylindrically shaped conductive liner with raised portions extending from the top edge of the conductive liner;

Figure 5D is a side view of a memory element incorporating

the electrical contact from Figure 5C;

Figures 6A-6S' is an embodiment of a process for making a memory element shown in Figure 5D;

Figure 7 is an example of a conductive liner with raised portions extending from a top edge of the liner's sidewall layers; and

Figure 8 is an example of an electrical contact having an increased resistivity in a region adjacent to the memory material.

Detailed Description of the Invention

The present invention is directed to programmable resistance memory elements. The memory element comprises a volume of memory material which is programmable between a first resistance state and a second resistance state in response to an electrical signal. The memory element further comprises a means of delivering the electrical signal to the volume of memory material. Preferably, the means of delivering the electrical signal comprises a first and a second electrical contact, also referred to as first and second electrodes, which are in electrical communication with the volume of memory material. The electrical contacts or electrodes do not have to be in physical contact with the memory material. (It is noted, that as used herein, the terminology "electrical contacts" and "electrodes" are synonymous and may be used interchangeably).

Figure 1A is an cross-sectional view of a memory device 100

formed on a semiconductor substrate 102. The cross-sectional view is parallel to the x-z plane. The y-z plane is perpendicular to the plane of the illustration of Figure 1A. In the example shown, the memory device 100 comprises two independent memory elements. The first memory element comprises a first electrical contact 130A (a bottom electrode), a layer of memory material 290 and a second electrical contact 300 (a top electrode). The second memory element comprises a first electrical contact 130B (a bottom electrode), a layer of memory material 290 and a second electrical contact 300 (a top electrode).

In the example shown, the volume of memory material is a substantially horizontally disposed layer of memory material 290. The memory material 290 and the second electrical contact 300 are shared by the first and second memory elements. However, other embodiments are possible where each memory element has a separate volume (or layer) of memory material and a separate second electrical contact. Dielectric regions 140 and 128 may be formed of silicon dioxide. Region 140 electrically isolates the bottom electrical contact 130A from the bottom electrical contact 130B. An upper dielectric region 180 is deposited on top of the memory device 100. The upper dielectric layer 180 may comprise boron-phosphate silica glass (BPSG). Reference to the electrical contact 130A,B refers to either electrical contact 130A or electrical contact 130B.

Each of the electrical contacts 130A and 130B shown in

Figure 1A is a conductive layer. More specifically, each is a conductive sidewall layer in the form of a conductive sidewall spacer. A conductive sidewall layer may be formed by the substantial conformal deposition of a conductive material onto a sidewall surface. In Figure 1A, sidewall surfaces 128S and bottom surface 106 form a trench extending perpendicular to the plane of the illustration.

In the example shown in Figure 1A, each conductive spacer 130A,B is "edgewise adjacent" to the memory material. That is, only edge 132 or a portion of edge 132 of conductive spacer 130A,B is adjacent to the memory material 290. The remainder of the conductive spacer is remote to the memory material. Hence, substantially all electrical communication between the conductive spacer 130A,B and the memory material 290 occurs through all or a portion of edge 132. It is noted that edge 132 does not have to be in actually physical contact with the memory material. Also, in an alternate configuration it is possible to position the layer 290 of memory material so that it is adjacent to an edge of only one of the conductive spacers.

Figure 1B is an idealized three-dimensional representation of conductive spacers 130A,B showing their thickness "t", width "w" and height "h". The thickness "t" of the conductive sidewall spacer 130A,B is the lateral dimension of the spacer along the x-axis dimension in the x-z plane (parallel to plane of the illustration). The thickness "t" of conductive sidewall spacer

130A,B may have a dimension which is smaller than what is producible by conventional photolithography. The width "w" is the lateral dimension of the conductive spacer along the y-axis in the y-z plane (perpendicular to the plane of the illustration of Figure 1A). The height "h" is the distance above the substrate 102.

As used herein the "area of contact" is the portion of the surface of an electrical contact through which the electrical contact electrically communicates with the memory material. While not wishing to be bound by theory it is believed that reducing the size of the area of contact reduces the volume of the memory material programmed, thereby reducing the total current needed to program the memory device.

As noted, in the embodiment shown in Figure 1A, substantially all electrical communication between the memory material 290 and conductive sidewall spacer 130A,B occurs through all or a portion of edge 132. Hence, the area of contact between the conductive spacer 130A,B and the memory material 290 is at least a portion of an edge the conductive sidewall spacer. The area of contact is thus very small and is proportional to the thickness of the conductive spacer adjacent to the memory material.

The area of contact may be reduced even further. In Figures 1A and 1B, each conductive sidewall spacer 130A,B has a substantially uniform width "w" (dimension of the spacer along the

y-axis). In order to further decrease the area of contact between each conductive sidewall spacer 130A,B and the memory material, each conductive sidewall spacer may be formed so that its width is reduced (i.e., the conductive spacer is made narrower) adjacent to the memory material. Reducing the width "w" of the sidewall spacer adjacent the memory material reduces the area of contact between the conductive spacer and the memory material. This embodiment, referred to as a "rapier" design of the conductive spacer, is shown in Figure 1C. Figure 1C is a cross-sectional view of a memory device 100' using a conductive sidewall spacer 130'A,B with a rapier design. The plane of the illustration is parallel to the y-z plane. As shown, the top edge 132 of the conductive sidewall spacer has been appropriately etched so that its width w is reduced adjacent to the memory material. In particular, each conductive spacer has been appropriately recessed to form a protrusion or raised portion 135 adjacent to the memory material. The raised portion 135 extends from the recessed edge 132' and terminates at a distal end or top surface 137 adjacent the memory material 290. The top surface 137 of the raised portion 135 is also referred to as the "tip" or "peak" of the raised portion. Figure 1D is a idealized three-dimensional representation of the conductive spacers 130'A,B having raised portions 135 that extend from the edges 132'. The top surface or tip 137 of each of the raised portions has a thickness "t" and a width "w2". The thickness "t" is the thickness of the conductive

layer 130'A,B adjacent to the memory material (not shown). Preferably, thickness "t" is less than about 750 Angstroms, more preferably less than about 500 Angstroms and most preferably less than about 300 Angstroms. The width "w2" of the raised portion 135 adjacent the memory material is less than the width "w1" of the sidewall layer 130'A,B adjacent the substrate 102. Preferably, the width "w2" is less than 700 Angstroms, more preferably less than 600 Angstroms and most preferably less than about 500 Angstroms. The thickness "t", the width "w2" as well as the surface area of the tip 137 may all be made smaller than what is permitted by photolithographic techniques. Preferably, the dimensions of the top surface 137 are sufficient so that the area of contact between the raised portion 135 and the memory material is preferably less than about 0.005 micron^2, more preferably less than about 0.0025 micron^2, and most preferably less than about 0.0015 micron^2.

The raised portion 135 may be made to have substantially vertical sidewalls (for example, substantially uniform width "w2" and substantially uniform thickness "t"), or it may be made to taper as it extends toward the tip 137 (for example, by tapering the width "w2 and/or by tapering the thickness "t"). Generally, the shape of the raised portion 137 is not limited to any particular shape. Examples of possible shapes include conical, pyramidal, prismatic and wedge-shaped frustums. The top surface or tip 137 of the raised portion 135 may be substantially flat or

rounded. It is also conceivable that the distal end or tip 137 may also be sharpened. The height of the raised portion 135 as well as the extent of any tapering may be controlled.

Referring again to Figure 1C, a dielectric material 145 is preferably positioned between the conductive sidewall layer 130'A,B and the memory material so that only the top surface 137 is exposed and in electrical contact with the memory material. Hence, substantially all electrical communication between each conductive layer 130'A,B and the memory material occurs through at least a portion of the top surface or tip 137 of the raised portion 135. The area of contact between each bottom electrode 130'A,B and the memory material is thus preferably defined by the top surface or tip 137. As noted above, in one embodiment of the invention it is preferable that the area of contact has an area less than about 0.005 micron^2, more preferably less than about 0.0025 micron^2, and most preferably less than about 0.0015 micron^2.

In an alternate embodiment of the invention, it is possible that the raised portion 135 be made to protrude into the memory material so that more of the surface of the raised portion 135 is in electrical contact with the memory material. It is noted that more than one raised portion may be formed on the edge 132' of each conductive layer 130'A,B.

The raised portions 135 may be made by forming a sidewall spacer over the conductive sidewall layers 130A,B that are shown

in Figure 1B. Specifically, the spacer is positioned above the conductive sidewall layers 130A,B where it is desired to position the raised portions 135. The spacer serves as a mask for either an anisotropic or isotropic etch. That is, the exposed sections of the edges 132 of the sidewall layers will be etched away and recessed while the section underlying the mask is at last partially protected from the etch so as to form raised portions or protrusions that extend from the recessed edges. Generally, the spacer which is used as the mask is not limited to any particular material. Preferably, the masking spacer is formed of a dielectric material such as an oxide or a nitride material. However, the masking spacer may also be formed of a semiconductor material such as a polysilicon. Moreover, it is also possible to form the masking spacer from a conductor such as aluminum. The spacer may be formed in many different ways.

An embodiment of a method for fabricating the memory device 100' of Figure 1C is shown in Figures 2A-2S. Referring first to Figure 2A, a substrate 102 is provided and a dielectric layer 128 is deposited on top of the substrate 102 to form the structure 200A shown in Figure 2A. The dielectric layer 128 may be a dielectric material such as silicon dioxide SiO_2 which may be deposited by means such as chemical vapor deposition (CVD).

Referring to Figure 2B, the dielectric layer 128 is then appropriately masked and etched to form a window or opening in the dielectric layer 128. The opening preferably exposes a portion of

the substrate (and preferably the exposed portion of the substrate is a conductive portion of the substrate). In the embodiment shown in structure 200B, the opening is a trench 170 which runs perpendicular to the plane of the illustration. The trench 170 has sidewall surfaces 128S (corresponding to the sidewall surfaces of the dielectric regions 128) and bottom surface 106.

A layer 133 of a conductive material is deposited onto the structure 200B to form the structure 200C shown in Figure 2C. Preferably, the deposition is a substantially conformal deposition. The layer 133 is deposited onto the top surfaces 128T of the dielectric regions 128, onto the sidewall surfaces 128S of the dielectric regions 128, and onto the bottom surface 106 of the trench 170. Hence, portions of the layer 133 are deposited along the two sidewall surfaces 128S of the trench 170. These portions of the layer 133 are sidewall layer portions 133S of the layer 133. The conformal deposition of layer 133 may be done using chemical vapor deposition techniques. Other possible deposition methods may be used as long as the sidewall surfaces 128S are appropriately covered by the layer 133.

Generally, the material 133 may be any conductive material. For example, it may be a metal, a metal alloy or a doped polysilicon. Examples of materials which may be used for layer 133 are include, but are not limited to, n-type doped polysilicon, p-type doped polysilicon, p-type doped silicon carbon alloys and/or compounds, n-type doped silicon carbon alloys and/or

compounds, titanium-tungstem, tungsten, tungsten silicide, molybdenum, and titanium nitride. Other examples include titanium carbon-nitride, titanium aluminum-nitride, titanium silicon-nitride, and carbon.

The n-type polysilicon may be formed "in situ" by depositing polysilicon in the trench 170 using a CVD process in the presence of phosphene. Alternately, the n-type polysilicon may be formed by first depositing polysilicon and then doping the polysilicon with phosphorous or arsenic. P-type doped polysilicon may be formed by first depositing polysilicon and then doping the polysilicon with boron.

Preferably, the thickness of layer 133 is between about 50 and about 1000 Angstroms, and more preferably between about 100 and about 500 Angstroms.

After the layer 133 is conformally deposited it is then anisotropically etched. The anisotropic etch removes those sections of the layer 133 which are substantially horizontally disposed and leaves those sections which are substantially vertically disposed. Specifically, the anisotropic etch removes the substantially horizontally disposed sections of the layer 133 that were deposited on top surfaces 128T of the regions 128. It also removes the substantially horizontally disposed section of the layer 133 deposited onto the bottom surface 106 of trench 170. The anisotropic etch leaves those sections of the layer 133 conformally deposited along the sidewall surfaces 128S. Hence,

the anisotropic etch leaves the sidewall layer portions 133S of the layer 133. The results of the anisotropic etch are shown as structure 200D in Figure 2D. The sidewall layer portions 133S of layer 133 form the conductive sidewall spacers 130A,B. The sidewall spacers 130A,B are formed having the top edges 132.

The conductive sidewall spacers 130A,B shown in Figure 2D extend continuously along the y-axis dimension of the trench 170 (that is, perpendicular to the plane of the illustration of Figure 2D). The next step in the process is to mask and etch the conductive sidewall spacers 130A,B so as to form a plurality of individual conductive sidewall spacers along the y-axis dimension of the memory array. These conductive spacers define individual memory elements along the y-axis dimension of the memory array.

The dielectric material, such a silicon dioxide is then deposited into the opening 170 and onto the sidewall spacers 130A,B. The dielectric material preferably fills the opening 170. Referring to Figure 140, it is seen that the dielectric material 140 is preferably deposited into the trench 170 and on top of the dielectric layers 128 of structure 200D to form structure 200E. The deposition may be done using a chemical vapor deposition process. The structure 200E may then chemically mechanically polished (CMP) or dry etched to form the structure 200F shown in Figure 2F. The chemical mechanical polishing or dry etching preferably planarizes the top surfaces of the sidewall layers 130A,B to expose at least a portion of one or both of the top

edges 132. In the embodiment shown in Figure 2F, at least a portion of each of the edges 132 is exposed. A three dimensional representation of the structure 200F is shown in Figure 2F'.

A first oxide layer 240 (for example, silicon dioxide from a TEOS source) is deposited onto the top surface of structure 200F to form the structure 200G shown in the three-dimensional representation of Figure 2G. Figure 2G' is a cross-sectional view of the same structure 200G parallel to the y-z plane and parallel to the width "w" of the sidewall spacer 130A,B. Preferably, the dimension of the first oxide layer 240 is between about 200 Angstroms and 500 Angstroms, and more preferably about 300 Angstroms. The first oxide layer 240 may be deposited using a chemical vapor deposition process. A layer 250 of polysilicon is then deposited on top of the oxide layer 240 to form structure 200H shown in the cross-sectional Figure 2H (parallel to the y-z plane) and in the three-dimensional representation of Figure 2H'. Preferably, the dimension of layer 250 is approximately 1000 Angstroms.

The structure 200H is then appropriately masked and etch. A layer of photoresist material is applied on top of the layer of polysilicon 250. The layer of photoresist is appropriately patterned (i.e., a pattern on a mask is transferred to the layer of photoresist) and a portion of the photoresist layer is removed to form the photoresist mask 260 shown in the three-dimensional view of Figure 2I. A top view of the structure 200I parallel to

the x-y plane is shown in Figure 2I'. Figure 2I' shows the relative positioning of the photoresist mask 260 relative to the top edges 132 of the conductive spacers 130A,B. A cross-sectional view of structure 200I, parallel to the y-z plan, is shown in Figure 2I''.

The structure 200I is then preferably dry etched to remove the portion of the polysilicon layer 250 which is not protected by the photoresist mask 260, thereby forming the structure 200J shown in Figure 2J. The etch used is selective to the oxide layer 240. The etch forms a sidewall surface 252 in the polysilicon layer 250. The photoresist 260 is then stripped from structure 200J to form structure 200K shown in Figure 2K.

A second oxide layer 270 (such as silicon dioxide) is then deposited onto the structure 200K to form the structure 200L shown in Figure 2L. Preferably, the layer 270 is deposited to a thickness of about 600 Angstroms. The second oxide layer 270 is deposited onto top horizontal surface of the polysilicon layer 250 as well as onto the exposed portion of the first oxide layer 240. It is also deposited along the sidewall surface 252 of the polysilicon layer 250. The oxide layer 270 is then anisotropically etched to remove the horizontally disposed portions of second oxide layer 270 and leave the vertically disposed portion 270A along the sidewall surface 252. The resulting structure is shown as structure 200M in Figure 2M. The remaining portion the oxide layer 270 is the portion 270A. The

portion 270A is a sidewall spacer.

The remaining portion of the polysilicon layer 250 shown in Figure 200M is then removed. This is preferably done by using a polysilicon dry etch. It is possible to use a wet polysilicon etch as well. The resulting structure is shown as structure 200N in Figure 2N. After this, the structure 200N is subjected to an anisotropic etch to remove the portions of the first oxide layer 240 that are not covered by the spacer 270A, leaving the oxide spacer 270B as shown by structure 200 O in Figure 2 O. A three dimensional representation of the structure 200 O is shown in Figure 2 O'. A top view (parallel to the x-y plane) of the oxide spacer 270B and its positioning relative to the top surfaces 132 of the conductive layers 130A,B is shown in Figure 2 O''. As seen, the spacer 270B overlies a portion of each of the exposed edges 132 of the sidewall spacers 130A,B. The "thickness" of the oxide spacer 270B (i.e. the spacer's lateral dimension in the y-axis dimension) is preferably smaller than which could be achieved though photolithographic methods (i.e., smaller than a photolithographic limit). In one embodiment, the thickness dimension of the oxide spacer 270B is preferably less 1000 Angstoms. In another embodiment, the thickness of the oxide spacer is preferably less than 700 Angstroms, more preferably less than 600 Angstroms and most preferably less than about 500 Angstroms.

Using the oxide spacer 270B as a mask, the conductive layers

are then etched to remove a portion of the conductive layers 130A,B and form raised portions underneath the spacer 270B. Referring to Figure 2P, at least a portion of each of the conductive layers not covered by the oxide spacer 270B is etched away and removed to form the recessed edges 132. However, at least a portion of each of the conductive layers covered by the oxide spacer 270B is at least partially protected from the etch to form the raised portions 135 that extend upwardly from the recessed edges. Figure 2P' is a cross-section view through a recessed conductive layer 130'A,B parallel to the y-z plane. The etch used may, for example, be a wet etch or a dry etch. Preferably, the etch used is a dry etch such as a plasma etch. The etch is preferably anisotropic so as to form raised portions 135 having substantially straight sidewalls. However, an isotropic etch may be used which removes a portion of the conductive material underneath the spacer and forms raised portions with sloped or tapered sidewalls. Hence, the raised portions 135 may be tapered (where the degree of tapering is controlled by the etching process used). Preferably, the raised portions 135 may have a height of about 500 Angstroms to about 2500 angstroms.

A layer 145 of a dielectric material (such as silicon dioxide) is then deposited onto the top of the structure 200P preferably by using conventional deposition methods (such as chemical vapor deposition) to form the structure 200Q shown in

Figure 2Q. The material is deposited into the recesses 138, onto the recessed edges and at least partially over the raised portions. The dielectric layer 145 and the oxide spacer 270B may then be chemically mechanically polished (CMP) to expose at least a portion of the top surface or tip 137 of each of the raised portions 135 and form the structure 200R shown in Figure 2R. (Of course, it may be possible to expose at least a portion of just one of the tips 137). A layer of memory material 290 and a second electrical contact 300 (i.e., a top electrode) are deposited on top of the structure shown in Figure 2R to form the memory element shown in Figure 2S.

It is noted that, after chemical mechanical polishing to form the structure 200R shown in Figure 2R (and before the deposition of the memory material), a barrier layer may, optionally, be formed on top of the structure 200R. (Hence, the barrier material would be formed between the tip (or top surface) 137 of the raised portion and the memory material). Barrier layer materials may be chosen to increase the conductivity between the electrical contact and the memory material, and/or improve the adhesion between the electrical contact and the memory material, and/or to prevent the electromigration of the electrical contact material into the memory material. Examples of certain barrier layer materials include, but are not limited to, titanium silicide, cobalt silicide and tungsten silicide.

Referring again to Figures 2P and 2P', it is again noted that

etching the conductive sidewall layers forms the narrow recesses 138 where the conductive layers are not underlying the oxide spacer 270B. After etching the conductive layers to form the recesses, it may be desirable to then etch the surrounding oxide regions 128 and 140 to the same level as the recessed edges 132' prior to depositing the dielectric layer 145 (as shown in Figure 2Q). This would eliminate the need for the dielectric material 145 to fill the narrow recesses 138. This would also make the subsequent chemical mechanical processing step (to get to the structure shown in Figure 2R) easier.

As shown above, the raised portions 135 may be made with the use of oxide spacers. As noted above, other materials may be used to form the spacers. In another embodiment of the present invention, the raised portions may be also made with nitride spacers that are preferably formed from silicon nitride. Referring Figures 2G through 2L, nitride spacers may be formed by replacing the first oxide layer 240 with a first silicon nitride layer, by replacing the polysilicon layer 250 with an oxide layer (such as silicon dioxide from a TEOS source) and by replacing the second oxide layer 270 with a second silicon nitride layer. The polysilicon etch (used to etch the polysilicon 250 as shown in Figures 2J and 2N) would be replaced with an oxide etch selective to an underlying silicon nitride material. Likewise, the oxide etch (used to anisotropically etch the oxide layers as shown in Figures 2M and 2 O) would be replaced with a silicon nitride etch.

More generally, the disclosed technique for forming raised portions above a conductive material should not be limited to the embodiments disclosed herein. The spacers may be formed using many different techniques. Also, the spacers may be formed from many different materials including dielectrics (for example, oxide and nitride), semiconductor materials (such as polysilicon) and conductors (such as aluminum). Likewise, the materials chosen for the layers 240, 250, 260 and 270 (as shown in the processing steps of Figures 2G through 2 O) are not limited to the embodiments provided and a wide range of materials may be used for each of the layers. The particular materials selected for each of the layers are preferably chosen to provide the proper selectivity during the various etching processes as will be recognized by persons of ordinary skill in the art.

As noted, the raised portions or protrusions as well the remaining conductive layer may be formed from any conductive material. Examples of materials include, but are not limited to, n-type doped polysilicon, p-type doped polysilicon, p-type doped silicon carbon alloys and/or compounds, n-type doped silicon carbon alloys and/or compounds, titanium-tungstem, tungsten, tungsten silicide, molybdenum, and titanium nitride. Other examples include titanium carbon-nitride, titanium aluminum-nitride, titanium silicon-nitride, and carbon.

In the embodiment of the memory device shown in Figure 2S,

the raised portion 135 extends from an edge of conductive layer 130'A,B. In the example shown, the conductive layer is a substantially planer, sidewall layer formed along the sidewall surface of a trench by depositing a layer of conductive material into the trench and then anisotropically etching the layer to remove the horizontally disposed surfaces.

More generally, raised portions may be formed on any conductive material having any physical geometry. In particular, in particular, raised portions or protrusions may be formed on an edge of any conductive layer (such as an conductive sidewall) having any physical geometry. Alternate forms of conductive sidewall layers may be made by the conformal deposition of a conductive material onto sidewall surfaces having various shapes and configurations. For example, a layer of conductive material may be substantially conformally deposited onto the sidewall surfaces of an opening (such as a via), a mesa or a pillar. The opening, mesa or pillar may be round, square, rectangular or irregularly shaped (likewise, the opening may be a trench). Anisotropically etching the conformally deposited conductive layer, removes the horizontally disposed portions of the deposited layer and leaves only one or more vertically disposed portions. The remaining one or more vertically disposed portions are sidewall layers in the form of conductive sidewall spacers having different shapes.

The sidewall spacer formed, for example, by the conformal

deposition of a conductive material into a circular opening (followed by an anisotropic etch) will be a conductive sidewall layer in the form of a cylindrical surface having two open ends. The top edge of the layer will be in form of an annulus. Changing the shape of opening (or pillar or mesa) will change the shape of the sidewall spacer. That is, the lateral cross section of the conductive sidewall spacer (i.e. the cross section parallel to the substrate) corresponds to the shape of the opening, mesa or pillar. Alternately, it may be rectangular or irregularly shaped.

Figure 3A shows a three-dimensional view of a cylindrical, conductive sidewall spacer 330 formed in a circular opening (and thus having a horizontal cross-section in the shape of an annulus). The cylindrical conductive spacer 330 comprises a single, cylindrically shaped sidewall layer. The thickness "t" of this cylindrically shaped sidewall layer is the distance between the inner and outer cylindrical surfaces as shown in Figure 3A. The cylindrical sidewall layer has two open ends or "rims" forming the top edge 332 and the bottom edge 331. The top and bottom edges 332 and 331 of the cylindrically shaped conductive sidewall layer 330 are annular surfaces formed by intersecting the conductive layer 330 with planes substantially parallel to the substrate. In the embodiment shown in Figure 3A, the layer of memory material 290 is adjacent only to the top end (i.e., the top edge 332) of the cylindrical sidewall spacer 330.

Substantially all electrical communication between the conductive spacer 330 and the memory material 290 is through the top edge 332 or a portion of the top edge 332. Hence, the area of contact between the conductive spacer 330 and the memory material 250 is the edge 332 or a portion of the edge 332. (That is, all or a portion of the annular surface 332).

The raised portions or protrusions may be formed atop the annular edge of a cylindrical sidewall layer. Figure 3B is a three-dimensional representation of a cylindrical conductive sidewall layer 330′ that includes raised portion or protrusions 335 that extend from the edge 332′. Each raised portion 335 extends from edge 332′ to an end or tip 337 adjacent the memory material (not shown). As noted above, the raised portions 335 are not limited to any particular shape. In the embodiment shown, the raised portions 335 have a thickness "t" (proportional to the thickness of the conductive layer) and a width "w". Conductive layer 330′ is in the form of a cylindrical conductive spacer. The raised portions may be formed on the top edge of the cylindrical conductive layer 330′ with the use of oxide spacers or nitride spacers as described above. An example of forming the raised portions atop the annular edge of a cylindrical sidewall layer will be given below. Preferably, substantially all electrical communication between the conductive spacer 330′ and the memory material is through one or more of the raised portions 335. More preferably, substantially all electrical communication between the

conductive spacer 330' and the memory material is through the upper surface or tip 337 of one or more of the raised portions 335. The electrical contact 330' and memory material may be positioned so that only all or a portion of the top end or tip 337 of one or more of the raised portions 335 are adjacent to the memory material while substantially all of the remaining portion of the electrical contact is remote to the memory material.

Figure 3C is a two dimensional side view of the cylindrical conductive layer 330', parallel to the x-z plane, showing the memory material 290 as well as the top electrical contact 300 (and also insulation materials 128, 140 and 180). In Figure 3C both of the raised portions 335 are in electrical communication with the memory material. However, it is also possible that the memory material and the raised portions 335 and the memory material be positioned relative to each other so that only one of the protrusions 335 is touching the memory material. In the embodiment shown in Figure 3C only the top surfaces or tips 337 are adjacent the memory material while the remainder of the electrical contact is remote to the memory material.

In the embodiments shown above, the conductive sidewall layers have been formed as conductive sidewall spacers. However, it is possible to form conductive sidewall layers in other ways. For example, a conductive sidewall layer may be formed as a portion of a "conductive liner". The conductive liner is preferably a single layer of conductive material deposited on the

sidewall surfaces as well as the bottom surface of a trench, opening (such as a via), or the like. Examples of conductive liners are shown in Figures 4A-C. In Figure 4A, the conductive liner 430A is formed in a trench. Figure 4B is an example of a conductive liner 430B formed in a rectangular opening. Figure 4C is an example of a conductive liner 430C formed in a circular opening (such as a circular via). Of course, other shapes are also possible. As shown in the Figures 4A-4C, each conductive liner has one or more sidewall layer portions as well as a bottom layer portion. The top end of the conductive liners is an open end having a top edge 432. (In the specific examples shown, the "top edge" 432 of each conductive liner is the surface formed by intersecting the respective conductive liner with a plane substantially parallel with the substrate 102). It is noted that the U-shaped conductive liner shown in Figure 4A has a "dual" top edge 432.

It is noted that in the examples of the conductive liners shown in Figures 4A-4C, the sidewall layer portions are substantially vertically disposed. However, this does not have to be the case. The sidewall layer portions may be tilted. This would be the case if the conductive liners were formed in either a trench or via having angled sidewall surfaces.

Figures 5A and 5B depict an embodiment of the memory element where the bottom electrical contact is a conductive liner 630

formed in a circular opening. Figure 5A is a three-dimensional view of the memory element while Figure 5B is a cross-sectional view parallel to the x-z plane. As seen, the conductive liner 630 is a cylindrical shell having an open top end (remote to and facing away from the substrate 102) and a closed bottom end (preferably adjacent to and in electrical communication with the substrate). The open top end has an annular top edge 632. The conductive liner 630 comprises a cylindrically shaped sidewall layer portion 630S and a bottom layer portion 630B.

In the example shown in Figures 5A and 5B, the conductive liner 630 is in the shape of a cylindrically shaped cup. As shown in Figure 5B, the sidewall layer portion 630S forms the side of the cup while the bottom layer portion 630B forms the bottom of the cup. The top edge 632 may be referred to as the "rim" of the cup. The conductive liner may have other cup shapes such as a paraboloid, hemisphere, cone, and frustum.

The layer 290 of memory material is preferably a planar, substantially horizontally disposed layer positioned adjacent to the open end (i.e., top edge 632) of the conductive liner 630. Hence, the memory material is adjacent only to the top edge 632 (i.e., the rim) of the conductive liner 630 or a portion of the top edge 532 of the conductive liner. The remainder of the conductive liner 630 is remote to the memory material. Preferably, substantially all electrical communication between the conductive liner 630 and the memory material occurs through the

edge 532 or a portion of the edge 632. Hence, the area of contact is defined by all or a portion of the edge 632. The edge 632 is an annulus having a thickness equal to the thickness of the conductive liner 630. The thickness of this annulus, and hence the area of contact between the conductive liner and the memory material may be reduced by decreasing the thickness of the conductive liner 630 deposited into the circular via. It is noted that it is possible that one or more intermediate layers be disposed between the memory material and the conductive liner.

One or more raised portions or protrusions may be formed on the top edge of the sidewall portion of a conductive liner. Figure 5C shows the cylindrical conductive liner 630' disposed on top of a substrate 102. In this embodiment, the conductive liner 630' includes at least one raised portion or protrusion 635. Each of the raised portions extends from the top edge 632' to a distal end or tip 637 (also referred to as a top surface) adjacent the memory material (the memory material is not shown in this diagram). In the embodiment shown, the raised portions 635 each have a thickness "t" (which is substantially the same as the thickness of the remainder of the conductive liner 630') and a width "w". Preferably, substantially all electrical communication between the conductive sidewall spacer 630' and the memory material is through one or more of the raised portions 635. More preferably, substantially all electrical communication between the

conductive spacer 630′ and the memory material occurs through the top surface or tip 635 of one or more of the raised portions 635. Hence, the electrical contact 630′ and memory material may be positioned so that only the top surface 637 of one or more of the raised portions 635 is adjacent to the memory material while substantially all of the remaining portion of the electrical contact is remote to the memory material.

Figure 5D shows a side view of a memory element, parallel to the x-z plane, made using the conductive liner 630′. Shown are memory material 290 and second electrical contact 300. In Figure 5D, the tips 637 of both protrusions 635 are in electrical contact with the memory material; however, it is possible that the memory material be positioned so that it is in electrical contact with only the upper surface 637 of only one of the protrusions 635. The base of the conductive liner 630′ is adjacent to and in electrical communication with the substrate 102.

The raised portions 635 may be formed with the use of sidewall spacers as described above. The sidewall spacers may be formed, for example, of oxide or silicon nitride. An embodiment of a method for fabricating the conductive liner 630′ is shown Figures 6A-6S′. Referring first to Figure 6A, a substrate 102 is provided and a dielectric layer 128 is deposited on top of the substrate 102. The dielectric layer may be formed from silicon dioxide and may be deposited by a chemical vapor deposition process. The dielectric layer 128 is then appropriately masked

and etched to form a window or opening in the form of opening 610 in the dielectric 128 as shown. The opening may be round, square, rectangular or irregularly shaped. Alternately, the dielectric layer 128 may be masked and etched to form a trench. Preferably, the opening (or trench) is made through the dielectric layer 128 to the substrate 102. In the embodiment shown in Figure 6A, the resulting structure 600A is a circular opening 610 which is formed in the dielectric 128. Figure 6B is a cross-sectional view (parallel to the y-z plane) of the three-dimensional structure 600A shown in Figure 6A. The sidewall surface 128S and the bottom surface 106 of the circular opening 610 is shown in Figure 6B. Preferably, the opening exposes at least a portion of the substrate.

A layer 633 of a conductive material is deposited on top of the structure shown in Figures 6A and 6B to form the structure 600C shown in Figure 6C. The layer 633 of conductive material is conformally deposited on top surfaces 128T of the dielectric region 128, on the sidewall surface 128S of the region 128 and the bottom surface 106 of the opening 640. Hence, the layer 633 has a top portion 633T, a sidewall layer portion 633S, and a bottom layer portion 633B.

A layer of dielectric material 140 (such as silicon dioxide) may then be deposited on top of the layer 633 so as to preferably fill the opening 610 and form the structure 600D shown in Figure 6D. The structure 600D may then be chemically mechanically

polished (CMP) or dry etched so as to planarize the top surface thereby removing a portion of layer 140 as well as the top layer portion 633T of the layer 633. The etch forms a cylindrical, cup-shaped conductive liner 630 having a sidewall layer portion 630S along the sidewall 128S and a bottom layer portion 630B along the bottom surface 106 as shown in Figure 6E. The etch also forms the edge 632. In the embodiment shown the edge 632 has the shape of an annulus. Preferably, the planarization step forms an edge which is substantially planar. Figure E′ shows a three-dimensional representation of the structure 600E from Figure 6E.

One or more raised portions or protrusions may be formed atop the edge 632. The processing steps for forming raised portions that extend from the top edge of the conductive liner are the similar to those described above with respect to the conductive sidewall spacers. A first oxide layer 640 is deposited on top of the conductive liner 600E to form the structure 600F shown in the three-dimensional representation of Figure 6F and in the cross-sectional view (parallel to the y-z plane) of Figure 6F′. A polysilicon layer 650 is deposited onto the first oxide layer 640 so form structure 600G as shown in Figures 6G and 6G′. A photoresist resist layer is deposited onto the polysilicon layer 650 and appropriately patterned to form photoresist mask 660 as shown in Figure 6H. A top view (parallel to the x-y plane) of the positioning of the photoresist layer 660 relative to the annular edge of the conductive cup 630 is shown in Figure 6H′. A cross-

sectional view (parallel to the y-z plane) is shown in Figure 6H''. The polysilicon layer 650 is appropriately patterned and etched to form a sidewall surface 652 in the layer 650 as shown in structure 600I of Figure 6I. The photoresist material is then removed as shown in Figure 6J. A second oxide layer 670 is conformally deposited over the top surface and the sidewall surface 652 of the remaining portion of the polysilicon layer 650 as well as over the top surface of the first oxide layer 640 as shown in Figure 6K. The horizontally disposed portions of the second oxide layer 670 are then removed preferably by an anisotropic etch of the oxide layer 670 leaving the vertically disposed oxide portion 670A along the sidewall surface of the polysilicon layer 650 as shown in Figure 6L. The remaining portion of the polysilicon layer 650 is then removed as shown in Figure 6M. The remaining oxide layer 640 and oxide portion 6A are then anisotropically etched to remove that portion of the oxide layer 640 that is not covered by the oxide spacer 670A. The remaining portion is the oxide spacer 670B shown in Figures 6N (parallel to the y-z plane) and 6N' (a three-dimensional view). Figure 6N'' is a top view parallel to the x-y plane of the structure 600N. As shown in Figure 6N'', the oxide spacer 670B is overlying a portion of the edge 632.

Using the oxide spacer 670B as a mask, the conductive layer 630 is then etched to form one or more raised portions underneath the spacer. Referring to Figure 6 O, at least a portion of the

conductive layer not covered by the spacer is etched away and removed to form a recessed edge 632'. However, at least a portion of the conductive layer covered by the oxide spacer 670B is at least partially protected from the etch to form the raised portions 635 that extend upwardly from the recessed edge. A side view (parallel to the y-z plane) of an etched conductive cup 630' having recessed edge 632' and raised portions 635 is shown in Figure 6P. Recession 638 is the gap formed between the oxide materials 128, 140 as a result of etching the conductive liner 630. As noted above, the etch may be anisotropic or isotropic. As well, the etch may be a dry etch or a wet etch.

An oxide layer 680 is then deposited into the recession 638 and on top of dielectric layers 128 and 140 as shown (as a cross-sectional view parallel to the y-z plane) in Figure 6Q. The oxide layer 680 and the oxide spacer 670B may then be chemically mechanically polished to expose at least a portion of the top surfaces or tips 637 of the raised portions 635 and to form structure 600R as shown in Figure 6R. A layer of programmable resistance memory material is disposed adjacent at least a portion of the raised portions. Referring to Figure 6S, a layer of memory material 690 is deposited on top of the structure 600R and, in particular, over at least a portion of one or both of the tips 627. A conductive layer 695 is deposited over the memory material 690 to form the upper electrode of the memory element 600S as shown in Figure 6S (a side view parallel to the y-z plane).

Figure 6S' shows an alternate side view of the structure 600S parallel to the x-z plane that shows the conductive liner 630' and both of the raised portions 635 with tips 637 adjacent the memory material 690. Only the top surfaces 637 of the raised portions 635 are adjacent to the memory material 690 while the remainder of the raised portions as well as the remainder of the conductive liner 630' is remote to the memory material 690. It is noted that the memory layer 690 may be positioned to that it is adjacent to only one of the raised portions 635.

It is noted, prior to the deposition of the oxide layer 680 shown in Figure 6Q it is possible to etch the dielectric regions 128 and 140 (shown in Figure 6P) to the level of the recessed edge 632'. This avoids the need to have the oxide material 680 fill the narrow gap 638 and also facilitates the chemical mechanical polishing. Also, as discussed above, it is possible to form protrusions 635 by using spacers formed from other dielectrics such as silicon nitride. Moreover, it is also possible to form spacers from semiconductor materials such as polysilicon or from conductors such as aluminum.

It is noted that in the embodiment of the method for forming the raised portion disclosed above, a sidewall spacer is used as a mask and a portion of the conductive material that does not underlie the mask (the sidewall spacer) is removed to form the raised portion. It is also possible that other types of masks may be used which are not sidewall spacers. For example different

types of patterned layers may be used as masks to form the raised portions. For example, it is possible that the patterned layers may simply be a portion of a layer (such as an oxide, nitride or polysilicon layer) which is formed on a portion of the edge of the conductive layer. Alternately, it is possible that the mask be a thin vertically disposed strip which is not formed as a sidewall layer.

A lateral dimension of the mask is a dimension of the mask as measured parallel to the substrate. For example, a lateral dimension may, for example, be the dimension of the mask as measured along either the x-axis or the y-axis when the substrate is parallel to the x-y plane. Preferably, at least one of the lateral dimensions of the mask is less than that which could be achieved through photolithography (i.e., it is less than a photolithographic limit). In one embodiment, at least one of the lateral dimensions is preferably less than about 1000 Angstroms. In another embodiment, at least one of the lateral dimensions is less than about 700 Angstroms, more preferably less than about 600 Angstroms, and most preferably less than about 500 Angstroms.

Likewise, other methods, besides the one presented above, may be used to form the masking sidewall spacers that are used to form the raised portions on the conductive materials. The methods and materials used depend, of course, on the underlying conductive material. For example, in an alternate method, a layer of polysilicon (a first layer) is deposited over the conductive

material. The layer of polysilicon is then be patterned and etched to form a sidewall surface. An oxide layer (a second layer) is then deposited onto the sidewall surface of the polysilicon. The oxide layer is anisotropically etched to remove the horizontally disposed surfaces and leave the sidewall spacer on the polysilicon. The polysilicon is then removed to leave only the oxide sidewall spacer that can now be used as mask. As described above, a portion of the conductive material not covered by the spacer is etched so as to form a raised portion extending from the conductive material under the spacer. The polysilicon and the oxide may, of course, be replaced with other materials. The materials chosen for the different layers (i.e., the first and second layers) depend upon the underlying conductive material and also upon the appropriate selectivity during the various etching processes. Still other methods known in the art may be used to form the masking spacers.

The raised portions or protrusions may be formed on an edge of the sidewall layers of different conductive liners. For example, they may be formed on the conductive liners shown in Figures 4A-4C. Figure 7 provides an example of a U-shaped conductive liner 720 that is formed in a trench. Figure 7 shows conductive liner 720 having two sidewall layer portions 730 and a bottom layer portion 740. The raised portions or protrusions 735 are formed on the edges 732 of the two sidewall layer portions 730 of the conductive liner 720. The protrusions 735 extend from the

edges 732 to tips 737. Substantially all of the electrical communication between the conductive liner 720 and the memory material (not shown) is preferably through one or both of the raised portions 735, and more preferably, through one or both of the top surfaces 737.

Hence, as disclosed above raised portions or protrusions may be formed on an edge of a conductive sidewall layer to form novel electrical contact structures. More generally, raised portions may be formed on the edge of any conductive layer having any shape or orientation. Still, more generally, one or more raised portions may be formed on any conductive material having any physical geometry.

In the memory devices discussed above, the electrical contacts deliver electrical current to the memory material. As the electrical current passes through the electrical contacts and through the memory material, at least a portion of the electric potential energy of the electrons is transferred to the surrounding material as heat. That is, the electrical energy is converted to heat energy via Joule heating. The amount of electrical energy converted to heat energy (that is, the amount of Joule heating) increases with the resistivity of the electrical contact (and memory material) as well as with the current density passing through the electrical contact and the memory material.

To increase the amount of heat energy transferred into the memory material, it may be possible to increase the resistivity of

the top surface or tip of the raised portion or protrusion that extends from the edge of the electrical contact. An example of this type of structure is shown in Figure 8. Figure 8 shows the conductive layer 130'A,B from Figure 1C where the protrusion 135 has a region R2 (adjacent the memory material) which has a higher resistivity than the region R1 remote to the memory material. U.S. Patent Application Serial No. 09/620,318 describes methods of making electrodes have two or more regions with different resistivities. The complete disclosure of U.S. Patent Application Serial No. 09/620,318 is hereby incorporated by reference herein.

The memory elements of the present invention may be electrically coupled to isolation/selection devices and to addressing lines in order to form a memory array. The isolation/addressing devices permit each discrete memory cell to be read and written to without interfering with information stored in adjacent or remote memory cells of the array. Generally, the present invention is not limited to the use of any specific type of isolation/addressing device. Examples of isolation/addressing devices include field-effect transistors, bipolar junction transistors, and diodes. Examples of field-effect transistors include JFET and MOSFET. Examples of MOSFET include NMOS transistors and PMOS transistors. Furthermore NMOS and PMOS may even be formed on the same chip for CMOS technologies.

Hence, associated with each memory element of a memory array

structure is isolation/addressing device which serves as an isolation/addressing device for that memory element thereby enabling that cell to be read and written without interfering with information stored in other adjacent or remote memory elements of the array.

The memory element of the present invention comprises a volume of memory material. Generally, the volume of memory material is a programmable resistance memory material which is programmable to at least a first resistance state and a second resistance state. The memory material is preferably programmed in response to electrical signals. Preferably, the electrical signals used to program the materials are electrical currents which are directed to the memory material.

In one embodiment, the memory material is programmable to two resistance states so that each of the memory elements is capable of storing a single bit of information. In another embodiment, the memory material is programmable to at least three resistance states so that each of the memory elements is capable of storing more than one bit of information. In yet another embodiment, the memory material is programmable to at least four resistance states so that each of the memory elements is capable of storing at least two bits of information. Hence, the memory materials may have a range of resistance values providing for the gray scale storage of multiple bits of information.

The memory materials may be directly overwritable so that

they can be programmed from any of their resistance states to any other of their resistance states without first having to be set to a starting state. Preferably, the same programming pulse or pulses may be used to program the memory material to a specific resistance state regardless of its previous resistance state. (For example, the same current pulse or pulses may be used to program the material to its high resistance state regardless of its previous state). An example of a method of programming the memory element is provided in U.S. Patent No. 6,075,719, the disclosure of which is incorporated by reference herein.

The memory material may be a phase change material. The phase-change materials may be any phase change memory material known in the art. Preferably, the phase change materials are capable of exhibiting a first order phase transition. Examples of materials are described in U.S. Patent Nos. 5,166,758, 5,296,716, 5,414,271, 5,359,205, 5,341,328, 5,536,947, 5,534,712, 5,687,112, and 5,825,046 the disclosures of which are all incorporated by reference herein.

The phase change materials may be formed from a plurality of atomic elements. Preferably, the memory material includes at least one chalcogen element. The chalcogen element may be chosen from the group consisting of Te, Se, and mixtures or alloys thereof. The memory material may further include at least one element selected from the group consisting of Ge, Sb, Bi, Pb, Sn, As, S, Si, P, O, and mixtures or alloys thereof. In one

embodiment, the memory material comprises the elements Te, Ge and Sb. In another embodiment, the memory material consists essentially of Te, Ge and Sb. An example of a memory material which may be used is $Te_2Ge_2Sb_5$.

The memory material may include at least one transition metal element. The term "transition metal" as used herein includes elements 21 to 30, 39 to 48, 57 and 72 to 80. Preferably, the one or more transition metal elements are selected from the group consisting of Cr, Fe, Ni, Nb, Pd, Pt and mixtures or alloys thereof. The memory materials which include transition metals may be elementally modified forms of the memory materials in the Te-Ge-Sb ternary system. This elemental modification may be achieved by the incorporation of transition metals into the basic Te-Ge-Sb ternary system, with or without an additional chalcogen element, such as Se.

A first example of an elementally modified memory material is a phase-change memory material which includes Te, Ge, Sb and a transition metal, in the ratio $(Te_aGe_bSb_{100-(a+b)})_cTM_{100-c}$ where the subscripts are in atomic percentages which total 100% of the constituent elements, wherein TM is one or more transition metals, a and b are as set forth herein above for the basic Te--Ge--Sb ternary system and c is between about 90% and about 99.99%. Preferably, the transition metal may include Cr, Fe, Ni, Nb, Pd, Pt and mixtures or alloys thereof.

A second example of an elementally modified memory material

is a phase-change memory material which includes Te, Ge, Sb, Se and a transition metal, in the ratio $(Te_aGe_bSb_{100-(a+b)})_cTM_dSe_{100-(c+d)}$ where the subscripts are in atomic percentages which total 100% of the constituent elements, TM is one or more transition metals, a and b are as set forth hereinabove for the basic Te-Ge-Sb ternary system, c is between about 90% and 99.5% and d is between about 0.01% and 10%. Preferably, the transition metal may include Cr, Fe, Ni, Pd, Pt, Nb, and mixtures or alloys thereof.

It is to be understood that the disclosure set forth herein is presented in the form of detailed embodiments described for the purpose of making a full and complete disclosure of the present invention, and that such details are not to be interpreted as limiting the true scope of this invention as set forth and defined in the appended claims.